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J1064 U.S. PTO 12/20/01

PTO/SB/05 (03-01)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	1248-CIC (P176US)
First Inventor	Kejariwal
Title	Non-invasive, Low Pin..Circ.& Methods
Express Mail Label No.	EU570627983US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [✔] Fee Transmittal Form (e.g., PTO/SB/17) *(Submit an original and a duplicate for fee processing)*
2. [ ] Applicant claims small entity status. See 37 CFR 1.27.
3. [✔] Specification [*Total Pages* 18] *(preferred arrangement set forth below)*
   - Descriptive title of the invention
   - Cross Reference to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. [✔] Drawing(s) *(35 U.S.C. 113)* [*Total Sheets* 8]
5. Oath or Declaration [*Total Pages* 6]
   a. [✔] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63 (d)) *(for continuation/divisional with Box 18 completed)*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. [✔] Application Data Sheet. See 37 CFR 1.76
7. [ ] CD-ROM or CD-R in duplicate, large table or Computer Program *(Appendix)*
8. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
      i. [ ] CD-ROM or CD-R (2 copies); or
      ii. [ ] paper
   c. [ ] Statements verifying identity of above copies

jc564 U.S. PTO 10/027187 12/20/01

ACCOMPANYING APPLICATION PARTS

9. [✔] Assignment Papers (cover sheet & document(s))
10. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
11. [ ] English Translation Document *(if applicable)*
12. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
13. [ ] Preliminary Amendment
14. [✔] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [✔] Nonpublication Request under 35 U.S.C. 122 (b)(2)(B)(i). Applicant must attach form PTO/SB/35 or its equivalent.
17. [✔] Other: Cert. of Mailing Express Mail

18. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:*

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No.: _____ / _____

Prior application information: *Examiner.* _____ *Group Art Unit:* _____

For CONTINUATION OR DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

19. CORRESPONDENCE ADDRESS

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Signature	James J. Murphy	*Date*	12-19-01

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FEE TRANSMITTAL for FY 2002

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT ($) 780.00

Complete if Known	
Application Number	
Filing Date	Dec. 20, 2001
First Named Inventor	Kejariwal
Examiner Name	
Group Art Unit	
Attorney Docket No.	1248-CIC (P176US)

METHOD OF PAYMENT

1. ☑ The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

Deposit Account Number: 23-2426

Deposit Account Name: Winstead Sechrest & Minick

☑ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

☐ Applicant claims small entity status. See 37 CFR 1.27

2. ☑ **Payment Enclosed:**

☑ Check ☐ Credit card ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	740	201	370	Utility filing fee	740.00
106	330	206	165	Design filing fee	
107	510	207	255	Plant filing fee	
108	740	208	370	Reissue filing fee	
114	160	214	80	Provisional filing fee	

SUBTOTAL (1) ($) 740.00

2. EXTRA CLAIM FEES

		Extra Claims		Fee from below	Fee Paid
Total Claims	20	-20** =	0	X	=
Independent Claims	3	- 3** =	0	X	=
Multiple Dependent					=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	84	202	42	Independent claims in excess of 3
104	280	204	140	Multiple dependent claim, if not paid
109	84	209	42	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0.00

***or number previously paid, if greater; For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for *ex parte* reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	920	217	460	Extension for reply within third month	
118	1,440	218	720	Extension for reply within fourth month	
128	1,960	228	980	Extension for reply within fifth month	
119	320	219	160	Notice of Appeal	
120	320	220	160	Filing a brief in support of an appeal	
121	280	221	140	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive - unavoidable	
141	1,280	241	640	Petition to revive - unintentional	
142	1,280	242	640	Utility issue fee (or reissue)	
143	460	243	230	Design issue fee	
144	620	244	310	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Processing fee under 37 CFR 1.17(q)	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	40.00
146	740	246	370	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	740	249	370	For each additional invention to be examined (37 CFR § 1.129(b))	
179	740	279	370	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	
Other fee (specify)					

*Reduced by Basic Filing Fee Paid **SUBTOTAL (3)** ($) 40.00

SUBMITTED BY				Complete *(if applicable)*	
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Signature	James J. Murphy			*Date*	12-19-01

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Attorney Docket No.
1248-CIC (P176US)

PATENT

CERTIFICATE OF MAILING BY "U.S. EXPRESS MAIL"
Under 37 C.F.R. 1.10(c)

"Express Mail" Mailing Label Number ___EM_570_627_983_US_
Date of Deposit December 20, 2001

This 18 pages of Application, 8 pages of Drawings, 6 page fully executed Declaration and Power of Attorney, along with Nonpublication Request PTO/SB/35 and fully executed Assignment, Assignment Cover Sheet and Assignment Recordal Fee check in the amount of $40.00 along with the PTO/SB17 Filling Fee Transmittal sheet for a LARGE ENTITY and check in the amount of $740.00 application fees, fully executed NonPublication Request Under 35 U.S.C.122(b) form PTO/SB/35 and Utility Patent Transmittal Form PTO/SB/05 with Certificate of Mailing and Application Data Sheet Information and return receipt post card are being deposited with sufficient postage with the United States Postal Service ""Express Mail Post Office to Addressee" service under 37 C.F.R. 1.10 on the date indicated above and is addressed to the Director of Patents, Box Patent Application, Washington, D.C. 20231.

S. Taylor Lenz

Signed Dec. 20, 2001

NON-INVASIVE, LOW PIN COUNT TEST CIRCUITS AND METHODS

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Approved for use through 10/31/2002. OMB 0651-0031
U.S. Patent and Trademark Office; U S DEPARTMENT OF COMMERCE

NONPUBLICATION REQUEST UNDER 35 U.S.C. 122(b)(2)(B)(i)

First Named Inventor	Kejariwal
Title	Non-invasive, Low Pin...Circuits & Methods
Atty Docket Number	1248-CIC (P176US)

I hereby certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing.

I hereby request that the attached application not be published under 35 U.S.C. 122(b).

12-19-01
Date

James J. Murphy
Signature

James J. Murphy, Esq. Reg. 34,503
Typed or printed name

This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application **upon filing.**

Applicant may rescind this nonpublication request at any time. If applicant rescinds a request that an application not be published under 35 U.S.C. 122(b), the application will be scheduled for publication at eighteen months from the earliest claimed filing date for which a benefit is claimed.

If applicant subsequently files an application directed to the invention disclosed in the attached application in another country, or under a multilateral international agreement, that requires publication of applications eighteen months after filing, the applicant **must** notify the United States Patent and Trademark Office of such filing within forty-five (45) days after the date of the filing of such foreign or international application. **Failure to do so will result in abandonment of this application (35 U.S.C. 122(b)(2)(B)(iii)).**

APPLICATION DATA SHEET

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Application Information:

Title: Non-Invasive, Low Pin Count Test Circuits and Methods
Classification: Class: Subclass:
Tech Center:
Drawing Sheets: 8 Drawing to be Published: __
Docket No: 1248-CIC (P176US)
Type: Utility
Secrecy: None

Representative Information:

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Domestic Priority: None CFR §119 Foreign Priority: None Filed on: n/a

Assignee: Cirrus Logic, Inc. 4210 South Industrial Boulevard, Austin, Travis County, Texas 78744

NON-INVASIVE, LOW PIN COUNT TEST CIRCUITS AND METHODS

[0001] FIELD OF INVENTION

[0002] The present invention relates in general to integrated circuits and in particular, to non-invasive, low pin-count test circuits and methods.

BACKGROUND OF INVENTION

[0003] Testing integrated circuits typically involves evaluation of important parameters at various functional levels under differing operating conditions, such as temperature. For example, the overall operation of the chip may be tested in addition to the specific testing of particularly critical circuits or circuit blocks. This is especially important with respects to complex integrated circuits where the overall device functionality may fall within specifications but the functioning of one or more internal circuit blocks is nonetheless only marginal.

[0004] The actual implementation of an efficient test protocol for a given chip is a non-trivial task subject to many variables. Among other things, if on-chip test circuitry is to be used, that test circuitry must be non-invasive. In other words, the operation of the test circuitry should not in itself alter any of the critical operating parameters of the device or disturb a critical signal path. Additionally, depending on packaging limitations, it is not always practical to provide sufficient pins for observing all the internal circuits requiring test. Further, notwithstanding the problem of access, some means must be provided to trigger the internal circuitry test mode. Finally, but of no less importance, some decision must be made as to which parameters and nodes are to be tested.

[0005] Given the importance of testing at various functional levels of an integrated circuit, improved testing techniques are required. These techniques should be non-invasive, neither disturbing critical signal paths nor dictating undue changes in the physical configuration device or packaging. They should be flexibly amenable to the testing of various nodes and parameters on the integrated circuit in a time-efficient fashion.

SUMMARY OF INVENTION

[0006] According to the principles of the present invention, methods and circuits are disclosed for the non-invasive testing of internal blocks of integrated circuits. According to one embodiment of these principles, a method is disclosed which includes steps of observing a selected parameter at a selected test node, detecting an error in response to the observation. Current to the integrated circuit stepped from a reference level by a selected current step representing the detected error.

[0007] The principles of the present invention have several advantages over the prior art. Among other things, by stepping the power supply current to the integrated circuit, more information can be transmitted in a non-invasive manner without the need for additional dedicated test pins. A number of different parameters can be tested and the results output while modulating the power supply current, including offset voltages. With respects to chopper stabilized amplifiers, an offset can be introduced into the amplifier input and the offset voltage at the output is observed. Moreover, the stepping of the power supply current can be used to time the counting of an oscillator output to verify proper oscillator operation.

BRIEF DESCRIPTION OF DRAWINGS

[0008] For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

[0009] FIGURE 1 is a functional block diagram of a multipath feedforward operational amplifier embodying the present inventive principles;

[0010] FIGURE 2 is a functional block diagram of one exemplary circuit for stepping the supply current to the operational amplifier of FIGURE 1 in response to selected test conditions;

[0011] FIGURE 3 is a timing diagram illustrating the typical operating regimes of the operational amplifier of FIGURE 1;

[0012] FIGURE 4A illustrates an exemplary power current profile illustrating the modulation of the power supply current during the test phase shown in FIGURE 3;

[0013] FIGURES 4B – 4F are voltage versus time diagrams of exemplary timing signals controlling the operating regimes of FIGURE 3 as generated by the state machine of FIGURE 1;

[0014] FIGURE 5 is an electrical schematic diagram of an exemplary power detect circuit suitable for generating the power detect control signal of Figure 4B;

[0015] FIGURE 6 is an electrical schematic of a selected one of the test circuit blocks shown in FIGURE 1;

[0016] FIGURE 7 is an electrical schematic diagram of an exemplary chopper-stabilized integrator suitable for use in selected ones of the integrator stages of FIGURE 1; and

[0017] FIGURES 8A and 8B are current profiles illustrating alternate methods of modulating the power supply current in response to selected test conditions.

DETAILED DESCRIPTION OF THE INVENTION

[0018] The principles of the present invention and their advantages are best understood by referring to the illustrated embodiment depicted in FIGURES 1 – 8 of the drawings, in which like numbers designate like parts.

[0019] FIGURE 1 is a functional block diagram of a feed-forward operational amplifier 100, fabricated on a single chip, and embodying the principles of the present invention. (Opamp 100 is only one of a number of possible applications of these principles, which are particularly useful in instances where testing of deeply embedded circuits is required and /or the number of pins or pads available for parameter observation is limited).

[0020] Opamp 100 is based on five (5) integrator stages 101a,e. In the preferred embodiment, integrator stage I1 is chopper-stabilized, as discussed in further detail below. A set of summers 102a,c implement the feed-forward function. The primary data path also includes ¼ attenuator 103 and 1/32 attenuator – low pass filter (LPF) 104.

[0021] According to the present inventive principles, three test blocks 105a,c are provided to monitor three selected nodes representing corresponding state variables in opamp 100. In the preferred embodiment, the data paths through opamp 100 are differential and test blocks 105a,c monitor the differential voltage between the conductor pairs, although other parameters can also be monitored. It should be noted that, electrical parameters such as voltage and current can also be monitored in embodiments using single-ended data paths. In the present example, when differential voltages exceeding a predetermined level are deemed to be an error and the supply current is modulated as a flag.

[0022] Timing and control of the chopper stabilization of integrator I1 and test block is effectuated with an on-chip oscillator 106. A state machine 107 generates the test control signals described in detail below.

[0023] A high-level functional block diagram of current modulation circuitry 200 which steps the supply current during test mode operations is shown as FIGURE 2. Conceptually, current modulation circuitry 200 comprises a plurality of parallel binary-weighted current sources 201a,d and associated loads 202a,d. Current source 201a is activated during the test mode calibration phase by the control signal CAL while current sources 201b,d are activated by the output signals from test blocks 105a, TESTMODE1 – TESTMODE3. Current sources 201a-d are deactivated in the normal mode, i.e., at the end of the test mode phase.

[0024] In the preferred embodiment, test mode operations are observed by monitoring power supply current. For this embodiment, the test mode phase is approximately 7 msec in duration and is divided into the time intervals shown in the timing diagram of FIGURE 3. During the first interval, of about 5 msec (i.e. between times t_0 and t_1, the internal circuits of op-amp 200 and the external testing instruments are allowed to stabilize to a steady state. This is followed by a second, calibration interval of approximately 2 msec. During the first 1 msec of the calibration interval, (i.e. between time t_1 and t_2.), the power supply current is stepped to a calibration current level. Then, in the last 1 msec of the calibration interval, (i.e. between time t_2 and t_3.), the power supply current is stepped as an indication of possible error locations.

[0025] An exemplary power current profile during test mode is shown in FIGURE 4A. The associated timing and control signals are shown in FIGURES 4B – 4F, where FIGURE 4B shows the power supply voltage profile, FIGURE 4B shows the signal Power_Detect ramping-up with the power supply, and

FIGURES 4C – 4F illustrate exemplary state machine – generated timing signals activating test blocks 105a,c and calibration current source 201a. Specifically, state machine output signal TESTMODE1 indicates that the test mode is active, CAL times the 2 msec calibration interval and TESTMODE2 times the final 1 msec during which detected errors are identified.

[0026] During the first 5 msec interval the current is higher than nominal since the test mode circuitry is running and therefore requiring power. This is followed by a step of 80 μamps of calibration current for 2 msec. As shown in FIGURE 2, the power supply current stepping is preferrably done by turning-on one or more parallel current sources 201. The calibration current is selected to provide a reference against which the error current steps are measured; if the calibration current source load varies from the specified nominal for a given device due to fabrication process variations, the error step current source loads on the same chip should vary similarly from their nominal values such that the absolute relationships between steps remains essentially the same.

[0027] In the last 1 msec of the test period, detected errors, if any, are flagged by an additional current step above the calibration level. In the present three test node example, binary weighted currents of 0, 40, 80 and 160 μamps are used to indicate the results, although other current magnitudes could be used depending on the particular application. The error step is the sum of the individual error currents representing each of the detected errors. For example, if two errors are detected, one represented nominally by 40 μamps and the other nominally by 160 μamps, then the total current step above the calibration level will be nominally 200 μamps. From the external observation point, a measured step of 200 μamps can be uniquely decoded as 40 and 160 μamp parts, representing the designated errors. If no error is detected, then the profile is

substantially flat after the 80 μamp calibration step. After the test mode is complete, the power supply current returns to its nominal state current requirement for normal mode functions.

[0028] Inducing the test mode when no extra pins are available for this purpose is another problem addressed by the inventive principles. There are a number of ways that this can be done. Preferably, a state machine is used which generates the control signals CAL, TESTMODE1 and TESTMODE2. The state machine is activated by power-detect circuitry 500 shown in FIGURE 5. Power-detect circuitry 500 generates a pulse when the power supply voltage exceeds a selected threshold, preferably 2vt of the transistors or approximately 1.4 volts.

[0029] While there are numerous parameters which can be tested in accordance with the inventive principles, the three parameters being tested are: (1) the differential voltages at three test nodes; (2) oscillator frequency; and (3) chopper operation.

[0030] In the illustrated embodiment, test blocks 105a,b preferably test the offset voltage at various points along the differential data path. One test block 105 is shown in further detail in FIGURE 6. (In this embodiment, , the same voltage detection circuit is used for each test node, although the comparator limits may differ).

[0031] Test circuitry 105 comprises a difference amplifier including a differential pair of transistors 601a,b responding to the input signals V_{IN}- and V_{IN}+ respectively and operating from a current source 603. Corresponding transistors 602a.b are biased such that they operate in the triode (non-saturation) region when transistors 601a,b have no differential input voltage (i.e. V_{IN}- = V_{IN}+). The common nodes represent the outputs TESTOUTM and TESTOUTP which have a low voltage swing of between 0.2 to 0.5 volts. The outputs of the difference amplifier

TESTOUTM and TESTOUTP, are input into a logic-OR gate 604 which generates TESTOUTX, where X is between 1 and 3 and represents the corresponding test block (node) 105a,c. A voltage difference between V_{IN}- and V_{IN}+ divides the current from current source unevenly between transistors 601a and 601b. The magnitude of the voltage difference at the gates of transistors 601a and 601b determines the direction and magnitude of the current split. In particular, if the difference between V_{IN}- and V_{IN}+ is sufficiently large, then most of the current is sunk through either transistor 601a or 601b and the corresponding voltage of TESTOUTP or TESTOUTM increases enough to cause OR gate 604 to generate the ultimate output signal TESTOUTX indicating an excessive imbalance at the node being tested.

[0032] In the preferred embodiment, each differential voltage detector is tuned by changing the current sources 603 and / or the sizes of transistors 601a,b.

[0033] Advantageously, the differential voltage detectors shown in FIGURE 6 sense node voltages without interfering with signal transmission through the tested nodes. Additionally, the preferred circuitry is turned-off (with the PDTEST signal) when the normal mode of operation begins.

[0034] The oscillator frequency is derived by a time measurement over the last 2 msec interval of the test mode. Specifically, the current steps at times t1 and t3 are used to define the 2 msec period over which counter 107 or similar circuit is used to count periods of the oscillator. The oscillator frequency can be derived from the time measurement between t1 and t3.

[0035] In the preferred embodiment of op-amp 100, integrator 101a (I1) is based on a chopper-stabilized amplifier as shown in FIGURE 7, where CMFB represent the common mode feedback. Chopper-stabilized amplifiers normally

chop their internal offsets. In other words, if a chopper-stabilized amplifier is working well, it should remove its internal offset. Hence, to test integrator I1 an offset V_{offset} is introduced at one of the integrator differential inputs pair transistor. If no difference is detected between the output offset voltage either during the 7 msec test mode or normal operation, then the chopper is functioning correctly.

[0036] It should be recognized that there are a number of alternate ways in which supply current can be modulated, two of which are shown in FIGURES 8A and 8B. Generally, the number of current levels needed to encode all possible error combinations is 2^n where n is the number of state variables to be monitored. In other words, when n increases the required levels increase exponentially, thus limiting n to 3 or 4.

[0037] In one alternate time-multiplexed encoding, n is divided into smaller numbers and then each number is encoded. For example if n is 4, the division can be made into two sequences and then each sequence coded as described above. The typically current waveform may look as shown in FIGURE 8A.

[0038] In another embodiment, pulse width modulation can be used to modulate power supply current with the code. Advantageously, this technique can be used to monitor a large number of state variables is short testmode times. If the number of state variables to be monitored is large, it can also be divided into smaller groups and a pulse width modulated sequence can be used for each number as shown in FIGURE 8B.

[0039] Additionally, there are alternate ways in which the test mode can be induced. In any event, the conditions or mechanism which induces self test mode should not be normally present or occurring during normal operation of the op amp. Moreover, the self test should last for a short time, in this example it lasts for 7milliseconds. In one alternate embodiment therefore, both the

differential input pins (INPUT, Fig. 1) are connected momentarily to 0.3volts below the lowest power supply voltage to the chip. Internally, a simple comparator circuit senses the voltage and it triggers the state machine as described above. (This voltage should be lower than the lowest power supply voltage but higher than -0.7volts at which voltage protection diodes at input pins start conducting and should not be asserted during normal operation).

[0040] A variation of this technique is to keep the input voltage lower for a specified time period. This makes accidental inducing of test mode more difficult.

[0041] Although the invention has been described with reference to a specific embodiments, these descriptions are not meant to be construed in a limiting sense. Various modifications of the disclosed embodiments, as well as alternative embodiments of the invention will become apparent to persons skilled in the art upon reference to the description of the invention. It should be appreciated by those skilled in the art that the conception and the specific embodiment disclosed may be readily utilized as a basis for modifying or designing other structures for carrying out the same purposes of the present invention. It should also be realized by those skilled in the art that such equivalent constructions do not depart from the spirit and scope of the invention as set forth in the appended claims.

[0042] It is therefore, contemplated that the claims will cover any such modifications or embodiments that fall within the true scope of the invention.

WHAT IS CLAIMED IS:

1. A method of testing an integrated circuit comprising the steps of:

observing a selected parameter at a selected test node;

detecting an error at the selected test node in responses to said step of observing; and

stepping a current to the integrated circuit from a reference level by a selected current step representing the detected error.

2. The method of Claim 1 and further comprising the steps of:

observing a selected parameter at a second selected test node;

detecting a second error in response to said step of observing the selected parameter at the second selected test node; and

stepping the current to the integrated circuit by a second selected step representing the second error, the current being a sum of the selected step and the second selected current step and representing the error and the second error.

3. The method of Claim 1 and further comprising the steps of:

allowing the current to settle to an initial level after initiation of a test mode; and

stepping the current to the reference level from the initial level.

4. The method of Claim 3 wherein the selected parameter comprises a differential voltage.

5. The method of Claim 2 wherein the selected step and the second selected step are binary weighted current steps.

6. The method of Claim 1 and further comprising the step of initiating a test mode in response to power-up of the integrated circuit.

7. A method of testing an integrated circuit including a plurality of test nodes comprising the steps of:

initiating a test mode;

during a first time interval of the test mode, stepping a level of a supply current of the integrated circuit to a calibration level;

observing parameters at the plurality of test nodes to detect errors;

during a second time interval of the test mode, selectively stepping the level of the supply current in response to a number of errors detected; and

decoding the level of the supply current to identify the detected errors.

8. The method of Claim 7 wherein said step of stepping the level of the supply current comprises the substeps of:

representing an error at each test node with a binary weighted current; and

selectively summing the binary weighted currents proportionate to the number of errors detected to generate a corresponding step of the level of the supply current.

9. The method of Claim 7 wherein said step of initiating comprises the step of initiating the test mode at power-up of the integrated circuit.

10. The method of Claim 9 and further comprising the step of allowing an initial current to the integrated circuit to settle during a third interval prior to the first interval of the test mode.

11. The method of Claim 7 wherein the integrated circuit operates in response to an oscillator output signal and said method further comprises the step of counting a number of periods of the oscillator output signal during the first and second intervals of the test mode.

12. The method of Claim 7 wherein said step of observing the parameters at the plurality of test modes comprises the substeps of:

introducing an offset at an input to a chopper stabilized amplifier forming a part of the integrated circuit; and

observing an offset voltage an output of the integrated circuit.

13. The method of Claim 7 wherein said step of observing comprises the substep of measuring a differential voltage offset at a selected one of the test nodes.

14. The method of Claim 11 and further comprising the step of stepping down the level of the supply current at the end of second interval, said step of measuring time period timed by said step of stepping the level of the supply current to the calibration level and said step of stepping down the level of the supply current at the end of the second interval.

15. An integrated circuit comprising:

a plurality of functional blocks each associated with a test node for observing an associated operating parameter;

detecting circuitry for detecting errors at said test nodes during a test mode; and

a plurality of parallel current sources for selectively stepping a supply current to said integrated circuit in response to errors detected by said detecting circuitry during said test mode.

16. The integrated circuit of Claim 15 wherein said plurality of parallel current sources are sized to selectively step said supply current in binary weighted steps.

17. The integrated circuit of Claim 15 wherein said detecting circuitry comprises a difference amplifier for monitoring a differential voltage at a selected one said test nodes.

18. The integrated circuit of Claim 15 further comprising a current source for selectively stepping said current to a calibration level during said test mode.

19. The integrated circuit of Claim 15 further comprising circuitry for initiating said test mode.

20. The integrated circuit of Claim 19 wherein said circuitry for initiating said test mode comprises voltage level detection circuitry for initiating said test mode on power-up of said integrated circuit.

NON-INVASIVE, LOW PIN COUNT TEST CIRCUITS AND METHODS

ABSTRACT:

[0043] A method of testing an integrated circuit including the steps of observing a selected parameter at a selected test mode to detect an error. The current to the integrated circuit is stepped from a reference level by selected amount.

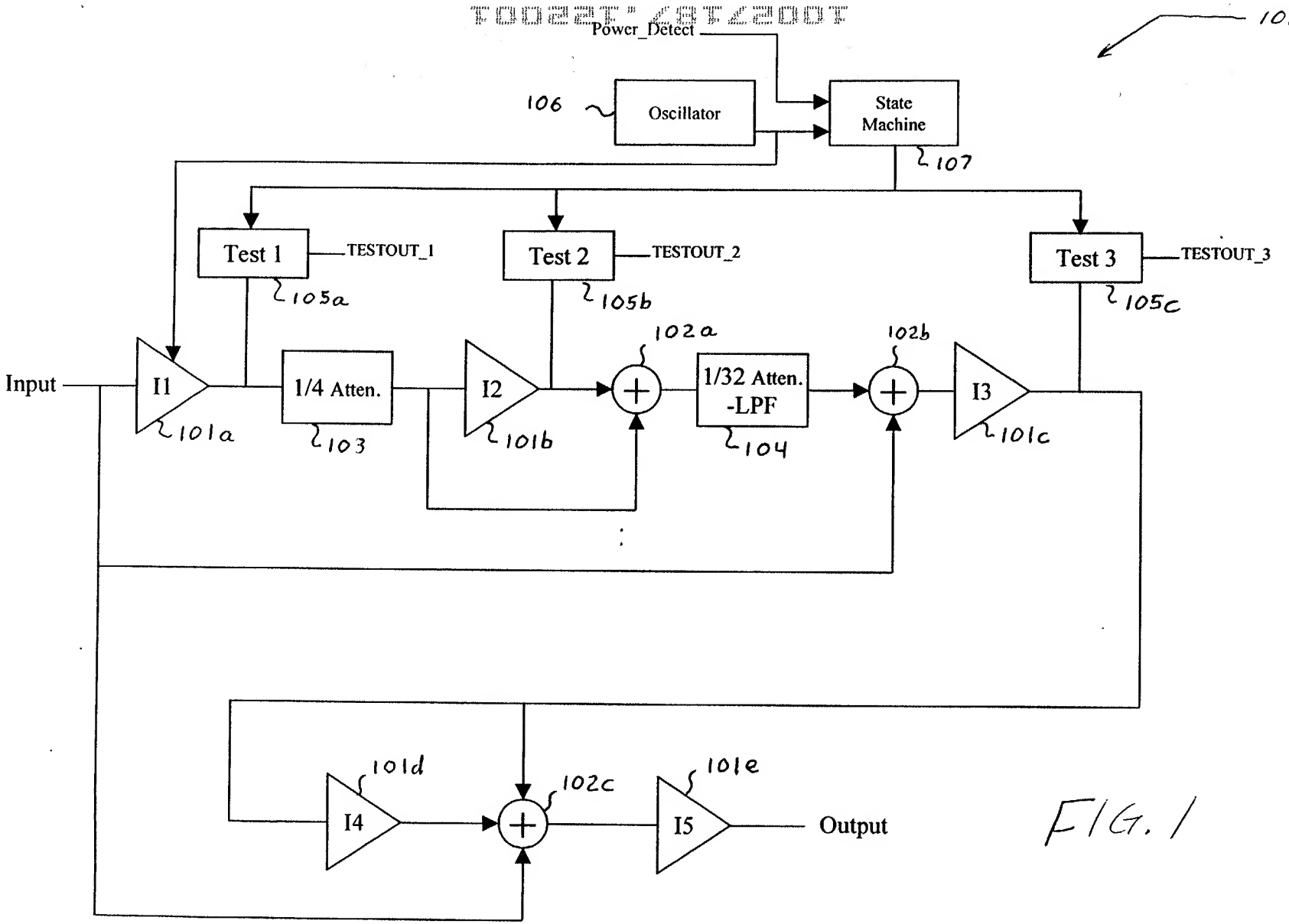


FIG. 1

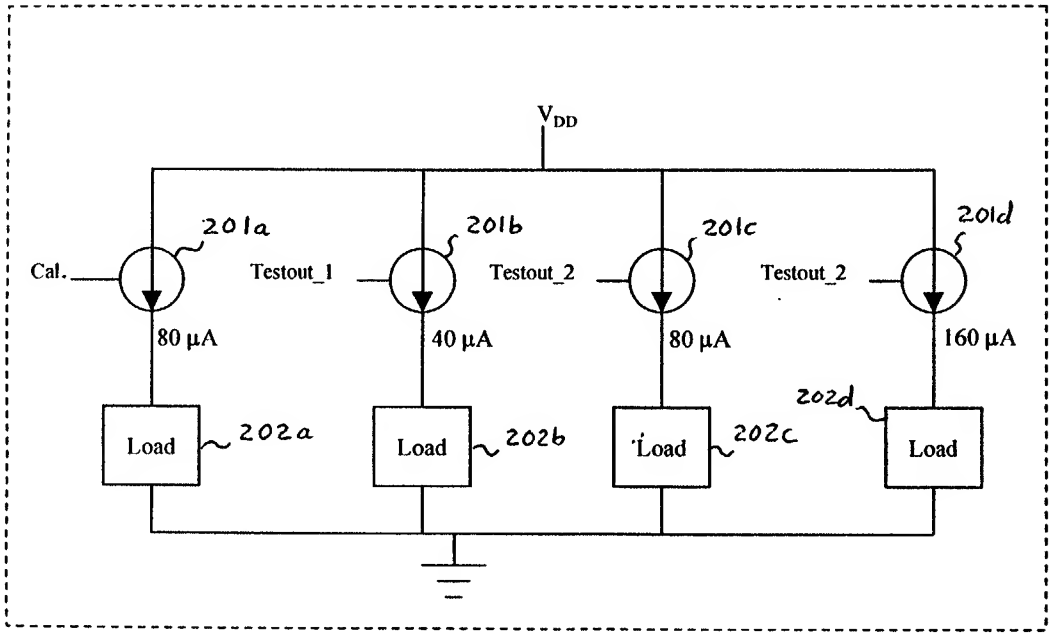

V_{DD}
201a
201b
201c
201d
Cal.
Testout_1
Testout_2
Testout_2
80 µA
40 µA
80 µA
160 µA
Load
202a
Load
202b
Load
202c
202d
Load

FIG 2

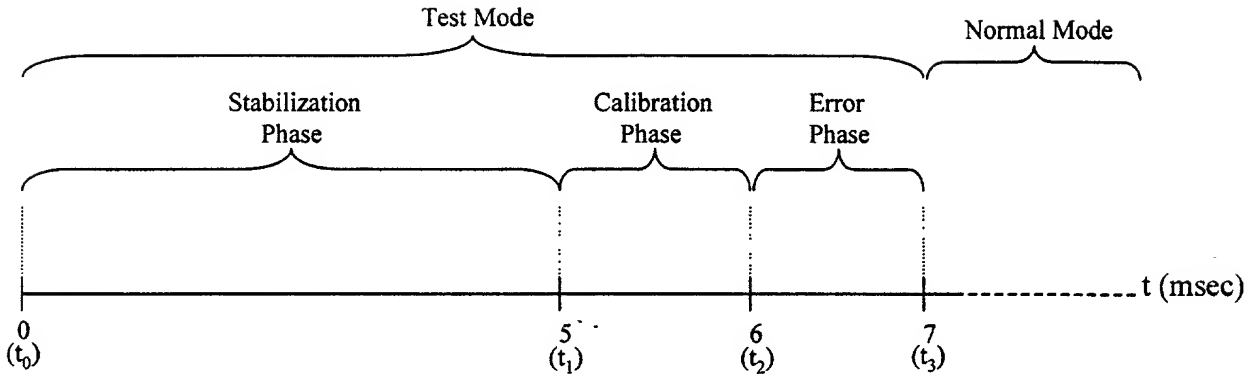

Test Mode
Normal Mode
Stabilization Phase
Calibration Phase
Error Phase
t (msec)
0 (t_0)
5 (t_1)
6 (t_2)
7 (t_3)

FIG. 3

Fig. 4B

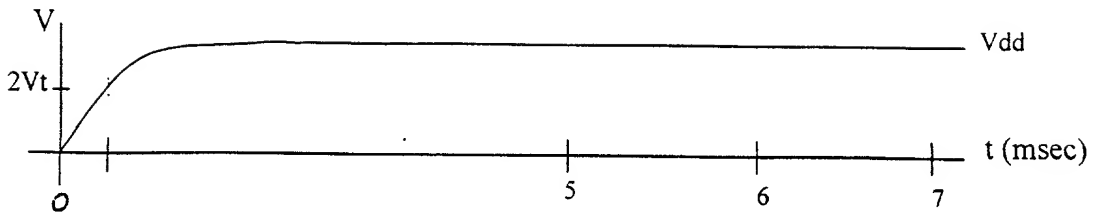


Fig 4C

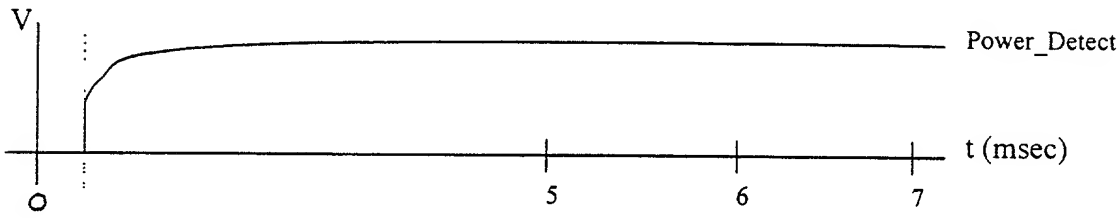


Fig 4D

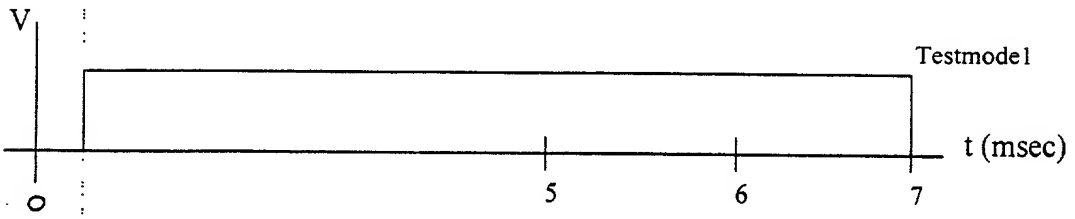


Fig 4E

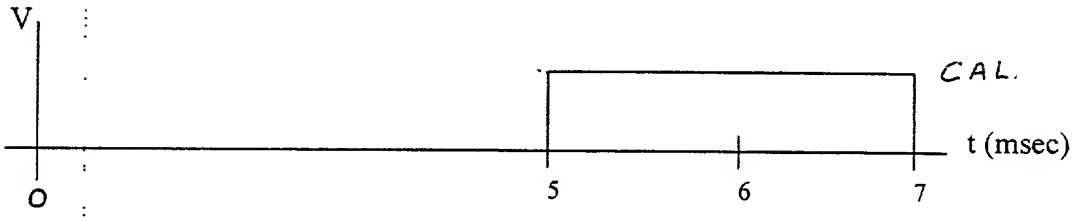
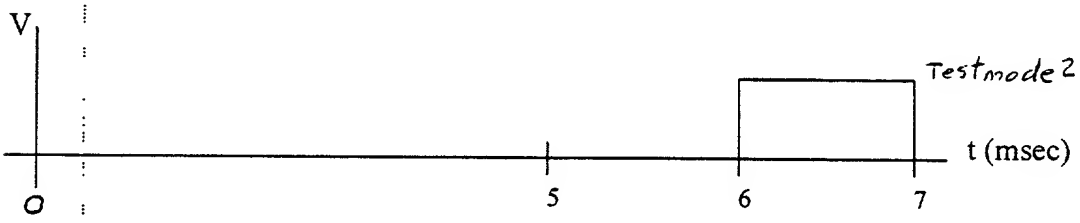


Fig 4F



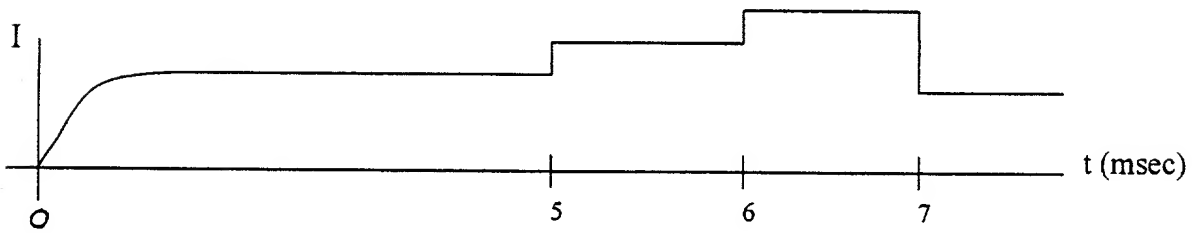


Fig. 4A

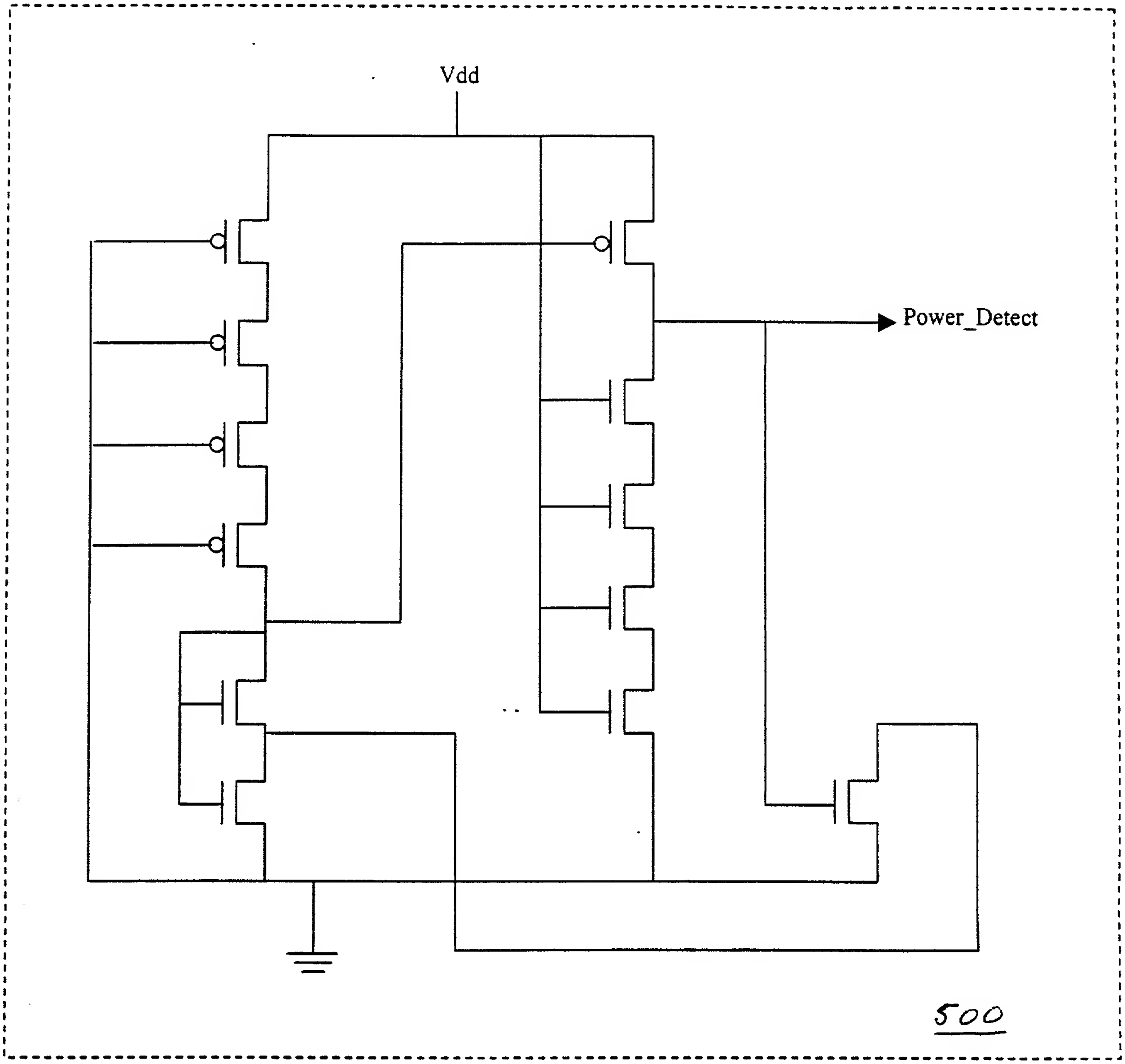
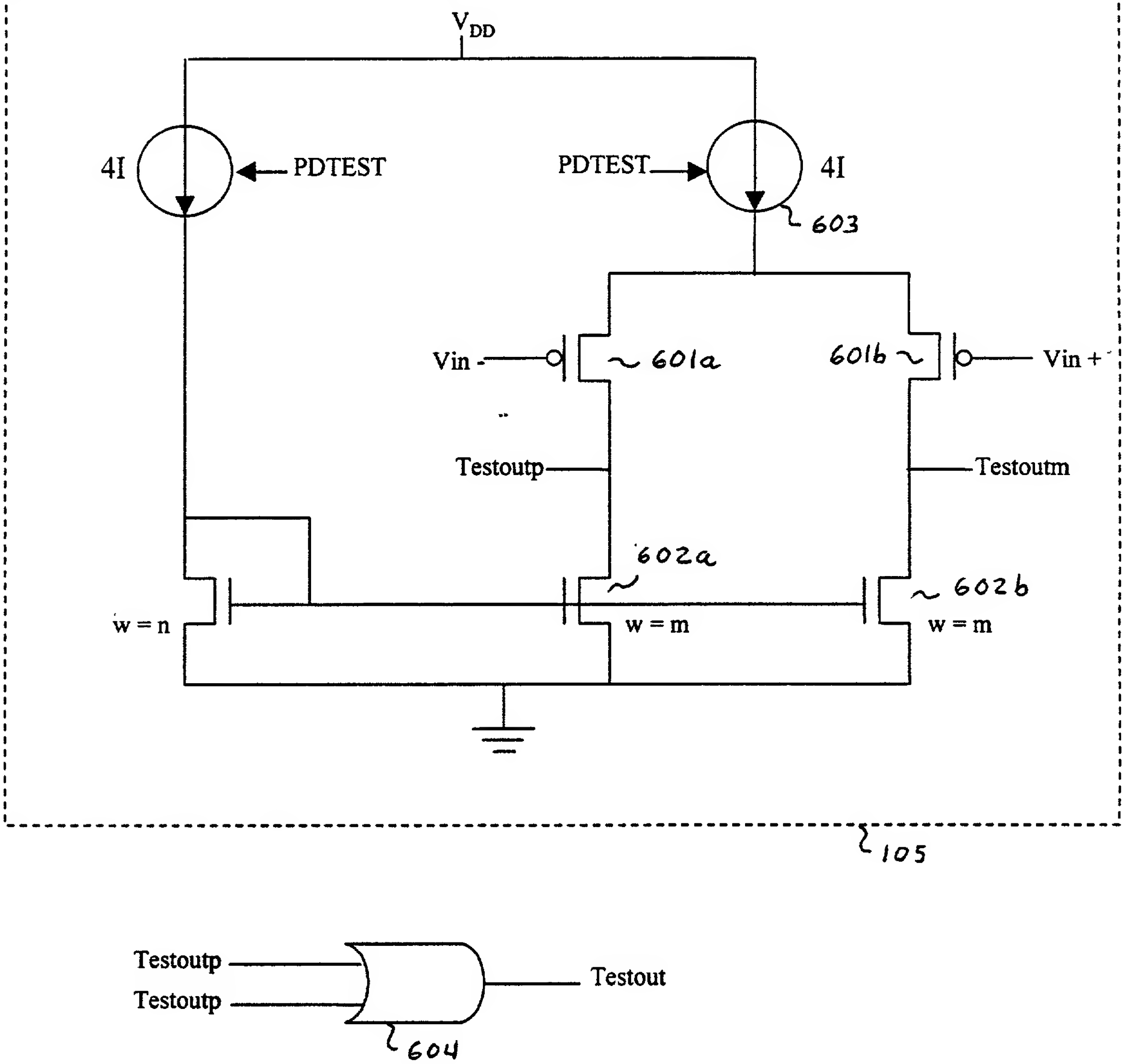


Fig 5



VDD
4I
PDTEST
PDTEST
4I
603
Vin -
601a
601b
Vin +
Testoutp
Testoutm
602a
602b
w = n
w = m
w = m
105
Testoutp
Testoutp
Testout
604

FIG. 6

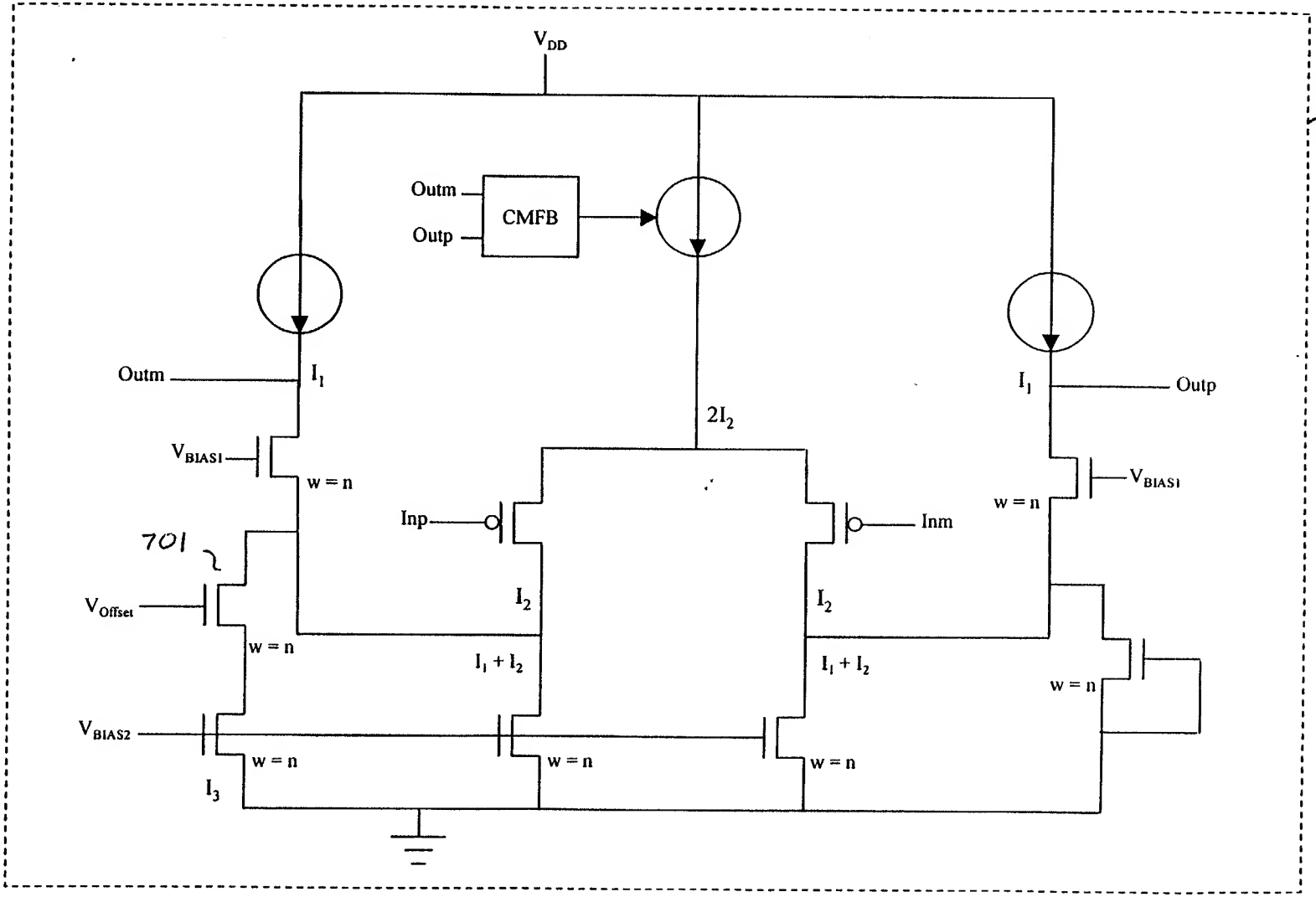

V_{DD}
101a
Outm
Outp
CMFB
Outm
I_1
V_{BIAS1}
w = n
701
V_{Offset}
w = n
V_{BIAS2}
w = n
I_3
Inp
Inm
$2I_2$
I_2
I_2
$I_1 + I_2$
$I_1 + I_2$
w = n
w = n
w = n
I_1
Outp
V_{BIAS1}
w = n
w = n

Fig 7

Fig 8A

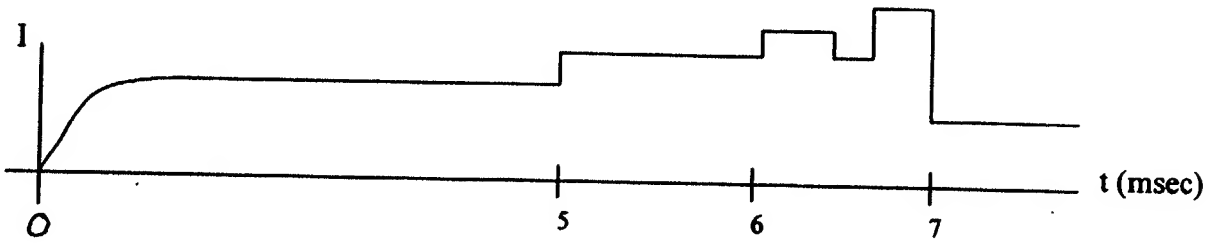
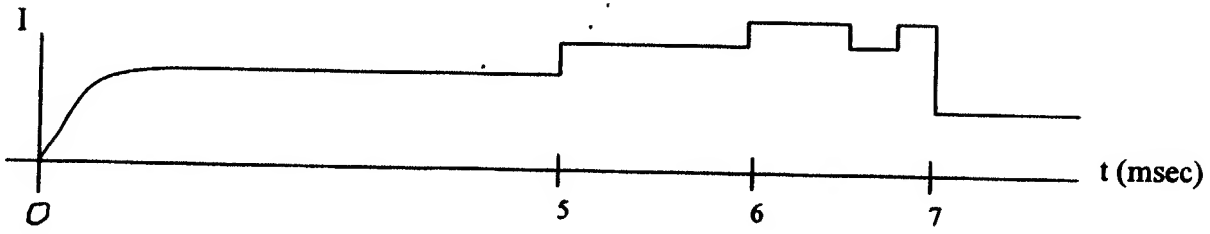


Fig. 8B



Attorney Docket Number
1248-CA

PATENT APPLICATION

DECLARATION AND POWER OF ATTORNEY
Original Application

As below named inventor, I declare that I have reviewed and understand the contents of the specification, including the claims, as amended by any amendment specifically referred to in this Declaration, that the information given herein is true, that I believe that I am the original, first and joint inventor of the invention entitled:

NON-INVASIVE, LOW PIN COUNT TEST CIRCUITS AND METHODS

which is described and claimed in:
XX the attached specification or
___ the specification in application Serial No. _____ filed _____
that I acknowledge my duty to disclose information in accordance with 37 C.F.R. Section 1.56 and defined on the attached sheet, which is material to the examination of this application, that I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof or patented or described in any printed publication in any country before my or our invention thereof, or more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months prior to this application and that as to applications for patent or inventor's certificate filed by me or my legal representatives or assigns in any country foreign to the United States of America, the earliest filed foreign application(s) filed within twelve months prior to the filing date of this application and all foreign applications filed more than twelve months prior to the filing date of this application, if any, are identified below.

CHECK APPROPRIATE BOX:

___ no earlier-filed foreign applications.
__ Required information as to foreign applications filed prior to the filing date of this application is on page __ attached hereto and made a part hereof.

POWER OF ATTORNEY:

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

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Attorney Docket Number
1248-CA

PATENT APPLICATION

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			USA

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

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Name (202)	Signature	Date
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Name (203)	Signature	Date
THOMSEN, Axel	Axel Thomsen	11/29/01
Name (204)	Signature	Date
MELANSON, John		3 Dec 01

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2836- P176S

Section 1.56 Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by Sections 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applications to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record of being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the application takes in:

(i) opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of patentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any considerations given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

© Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent or inventor.

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